CLAIMS

What is claimed is:

- A method of erasing a logical data block of a magnetic random access
 memory (MRAM), the method comprising:
 providing a MRAM having a logical data block configured for a distribution of selected and unselected write field thresholds when switching from a logical one state to a logical zero state, wherein the selected write field threshold is separated from the unselected write field threshold by a preselected amount; and
- writing all bits of the logical data block to the logical one state.
 - 2. The method of claim 1, wherein the providing a MRAM having a logical data block comprises providing a MRAM, wherein the logical data block comprises: a plurality of magnetic memory cells;
- an easy-axis conductor configured for generating an easy-axis magnetic field, operably coupled to a first side of each of the plurality of magnetic memory cells; and a plurality of hard-axis conductors configured for generating a hard-axis magnetic field operably coupled to a second side of each of the plurality of magnetic memory cells.
- 3. The method of claim 1, wherein the preselected amount provides fewer bit errors than the maximum number of bit errors that is correctable by a preselected error correction code.
- The method of claim 3, wherein the preselected error correction code
 comprises at least one of Bose-Chaudhuri-Hochquenghem code, Reed-Solomon code and run length limited code.
 - 5. The method of claim 3, wherein the preselected amount comprises a predetermined number of standard deviations difference from a mean of the unselected write field distribution to a maximum switching field in an easy-axis magnetic field.
 - 6. The method of claim 1, wherein writing all bits of the logical data block further comprises using only easy-axis write current.

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7. A method of writing a logical data block of a magnetic random access memory (MRAM), the method comprising:

providing a MRAM having a logical data block configured for a distribution of selected and unselected write field thresholds when switching from a logical one state to a logical zero state, wherein the selected write field threshold is separated from the unselected write field threshold by a preselected amount;

writing all bits of the logical data block to the logical one state; and writing the logical zero state into selected target bits of the logical data block.

10 8. The method of claim 7, wherein having the logical data block further comprises:

magnetic memory cells;

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an easy-axis conductor configured for generating an easy-axis magnetic field, operably coupled to a first side of each of the magnetic memory cells; and a plurality of hard-axis conductors configured for generating a hard-axis magnetic field

operably coupled to a second side of each of the magnetic memory cells.

- 9. The method of claim 7, wherein the preselected error correction code comprises at least one of Bose-Chaudhuri-Hochquenghem code, Reed-Solomon code and run length limited code.
- 10. A magnetic random access memory (MRAM), comprising a logical data block configured for a distribution of selected write field thresholds and unselected write field thresholds when switching from a logical one state to a logical zero state, wherein the distribution of selected write field threshold is separated from the distribution of unselected write field threshold by a preselected amount.
- The MRAM according to claim 10, wherein the logical data block comprises: an easy-axis conductor configured for generating an easy-axis magnetic field;
 a plurality of hard-axis conductors configured for generating a hard-axis magnetic field; and magnetic memory cells formed at intersections of the easy-axis conductor and the plurality of hard-axis conductors.

- 12. The MRAM according to claim 11, wherein the easy-axis conductor comprises a row conductor.
- 13. The MRAM according to claim 11, wherein the easy-axis conductor comprises a write line.
 - 14. The MRAM according to claim 11, wherein the plurality of hard-axis conductors comprise column conductors.
- 10 15. The MRAM according to claim 11, wherein the plurality of hard-axis conductors comprise bit lines.
- The MRAM according to claim 11, wherein the magnetic memory cells comprises at least one of a giant magnetoresistance (GMR) device, a tunneling
 magnetoresistance (TMR) with magnetic tunnel junction (MJT) device, a diode-isolated MTJ device, a transistor-isolated MJT device, a Hall effect storage device and a ballistic tunneling device.
 - 17. A magnetic memory module, comprising:
- at least one magnetic random access memory (MRAM) comprising at least one logical data block configured for a distribution of selected and a distribution of unselected write field thresholds when switching from a logical one state to a logical zero state; the distribution of the selected write field threshold configured for separation from the distribution of the unselected write field threshold by a preselected amount; and an input/output interface in communication with the at least one MRAM for communicating with external circuitry.
 - 18. The magnetic memory module according to claim 17, wherein the at least one logical data block, comprises:
- an easy-axis conductor configured for generating an easy-axis magnetic field;
 hard-axis conductors configured for generating a hard-axis magnetic field operably coupled
 to a second side of each of the plurality of; and
 magnetic memory cells formed at intersections of the easy axis conductor and the hard axis

magnetic memory cells formed at intersections of the easy-axis conductor and the hard-axis conductors.

19. A computer system, comprising:

an input device;

an output device;

a processor operably coupled to the input device and the output device; and
a memory device operably coupled to the processor, the memory device comprising:
at least one magnetic random access memory (MRAM) comprising at least one
logical data block having a distributions of selected and unselected write field
thresholds when switching from a logical one state to a logical zero state, the
distribution of the selected write field threshold configured for separation from

amount; and

an input/output interface in communication with the at least one MRAM for communicating the processor.

the distribution of the unselected write field threshold by a preselected

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20. The computer system according to claim 19, wherein the at least one logical data block, comprises:

an easy-axis conductor configured for generating an easy-axis magnetic field, operably coupled to a first side of each of a plurality of magnetic memory cells; and a plurality of hard-axis conductors configured for generating a hard-axis magnetic field operably coupled to a second side of each of the plurality of magnetic memory cells.